AT30TS01

±0.5°C Accurate, 1.7V Digital Temperature Sensor

DATASHEET

Features

- Low Power I^2C Digital Temperature Sensor
- JEDEC JC42.4 Component Specification Compliant
- Low Voltage Operation
  - Optimized for V_{CC} range of 1.7V to 3.6V
- 2-wire Serial Interface: I^2C Fast Mode Plus (FM+) Compatible
  - 100kHz, 400kHz, and 1MHz Compatibility
  - Bus Timeout Supported
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Industry Standard Green (Pb/Halide-free/RoHS compliant) Package Option
  - 8-pad Very Very Thin DFN (2.0 x 3.0 x 0.8mm)

Temperature Sensor Features

- Measures Temperature From -40°C to +125°C
- Temperature Converted to Digital Data with 12-bit Resolution
- Highly Accurate Temperature Measurements Requiring No External Components
  - ±0.5°C/ ±1.0°C Accuracy (typ/max) Over the +75°C to +95°C Range
  - ±1.0°C/ ±2.0°C Accuracy (typ/max) Over the +40°C to +125°C Range
  - ±2.0°C/ ±3.0°C Accuracy (typ/max) Over the -20°C to +125°C Range
- Programmable Hysteresis Threshold: Off, 0°C, 1.5°C, 3.0°C, and 6.0°C
- Low Operating Current
  - Temperature Sensor Active ~0.2mA (Typical)

Typical Applications

- Temperature Sensing for Solid State Drive (SSD)
- Internet of Things Wearable Devices
- Servers, Laptops, and PC Boards
- Handheld/Portable Devices
- PC Peripherals
- Medical Consumables
- Industrial Applications
- Consumer Electronics
- General Purpose Temperature Monitoring

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1. Description

The Atmel® AT30TS01 is a digital temperature sensor device with accuracy up to ±0.5°C designed to target low voltage (1.7V V_{CC} or higher) applications that require the highest level of temperature readout. The AT30TS01 is fully compliant with the JEDEC JC42.4 Component Specification.

The AT30TS01 continuously monitors temperature and updates the data in the temperature register, and the temperature data is latched internally by the device and may be read by software via a bus Master at anytime.

The AT30TS01 incorporates several user programmable internal registers to configure and optimize the temperature sensor's performance to provide maximum flexibility for temperature sensing applications. The device contains flexible programmable high, low, and critical temperature limits. The result of the digitized temperature measurements are stored in one of the AT30TS01 internal registers, which is readable at any time through the device's serial interface. The $\overline{\text{EVENT}}$ pin is an active low output and can be configured to operate as an Interrupt or as a Comparator output. The Manufacturer and Device ID Registers provide the ability to confirm the identity of the device. The AT30TS01 supports the industry standard 2-wire I^2C FM plus (Fast Mode +) serial interface allowing device communication to operate up to 1MHz. A bus timeout feature is supported to help prevent system lock-ups.

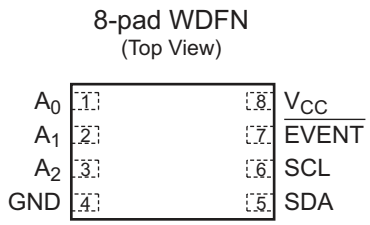
The AT30TS01 is factory-calibrated and requires no external components to measure temperature. With its flexibility and high-degree of accuracy, the AT30TS01 is ideal for extended temperature measurements in a wide variety of communication, computer, consumer, environmental, industrial, and instrumentation applications. The AT30TS01 is available in a space saving WDFN package.

2. Pin Descriptions and Pinout

Table 2-1. Pin Descriptions

Symbol	Name and Function	Asserted State	Type
SCL	**Serial Clock:** The SCL pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is always clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled-high using an external pull-up resistor.	—	Input
SDA	**Serial Data:** The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled-high using an external pull-up resistor (not to exceed 8KΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.	—	Input/ Output
EVENT	**EVENT:** The $\overline{\text{EVENT}}$ pin is an open-drain output pin used to indicate when the temperature goes beyond the user-programmed temperature limits. The $\overline{\text{EVENT}}$ pin can be operated in one of three different modes; Interrupt, Comparator, or Critical Alarm Modes. The ALERT pin must be pulled-high using an external pull-up resistor for proper operation.	—	Output
A_2, A_1, A_0	**Device Address Inputs:** The A_0, A_1, and A_2 pins are used to select the Device Address and corresponds to the three Least-Significant bits (LSb) of the I^2C FM+ seven bit slave address. These pins can directly be connected to V_{CC} or GND in any combination, allowing up to eight devices on the same bus.	—	Input
V_{CC}	**Device Power Supply:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.	—	Power
GND	**Ground:** The ground reference for the power supply. GND should be connected to the system ground.	—	Power

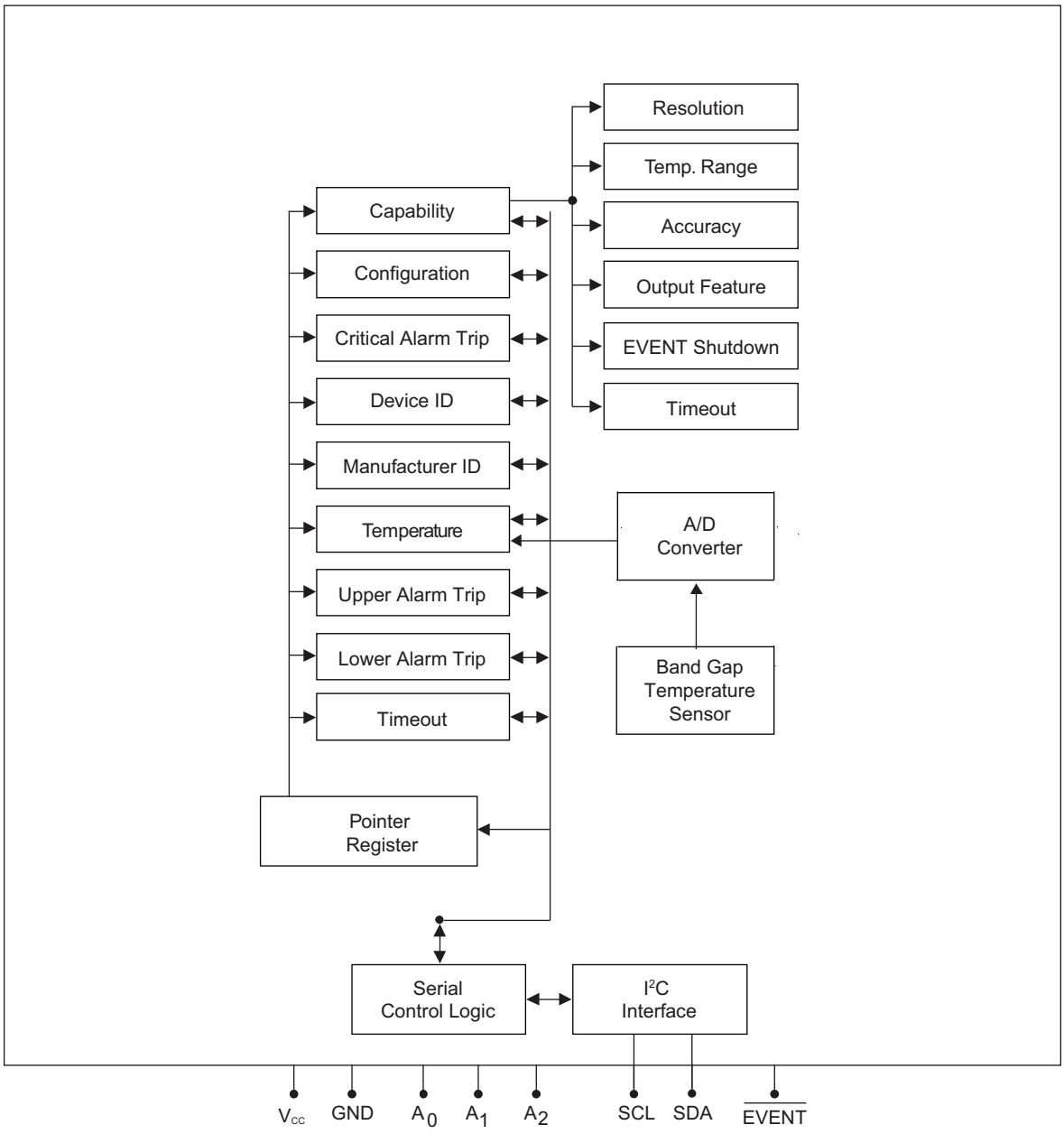
Figure 2-1. Pinout



Note: The metal pad on the bottom of the WDFN package is not internally connected to a voltage potential. This pad can be a “no connect” or connected to GND.

3. Block Diagram

Figure 3-1. Block Diagram



4. Device Communication

The AT30TS01 operates as a slave device and utilizes a simple 2-wire digital serial interface compatible with the I^2C Fast Mode Plus (I^2C FM+) protocol to communicate with a host controller commonly referred to as the bus Master. The Master initiates and controls all Read and Write operations to the slave devices on the serial bus, and both the Master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: the Serial Clock (SCL) and the Serial Data (SDA). The SCL pin is used to receive the clock signal from the Master, while the bidirectional SDA pin is used to receive command and data information from the Master, as well as, to send data back to the Master. Data is always latched into the AT30TS01 on the rising edge of SCL and is always output from the device on the falling edge of SCL. Both the SCL and SDA pin incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most-Significant Bit (MSB) first. During the bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data have been transferred, the receiving device must respond with either an acknowledge (ACK) or a no-acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the Master; therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any Read or Write operation so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the Master and the slave devices.The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the Master.

In order for the serial bus to be idle, both the SCL and SDA pins must be in the Logic 1 state at the same time.

4.1 Start Condition

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is stable in the Logic 1 state. The Master uses a Start condition to initiate any data transfer sequence, and the Start condition must precede any command. AT30TS01 continuously monitors the SDA and SCL pins for a Start condition, and the device does not respond unless one is given. Please refer to Figure 4-1 on page 7 for more details.

4.2 Stop Condition

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the Logic 1 state. The Master uses the Stop condition to end a data transfer sequence to the AT30TS01 which subsequently returns to the idle state. The Master can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the Master performs another operation. Please refer to Figure 4-1 on page 7 for more details.

4.3 Acknowledge (ACK)

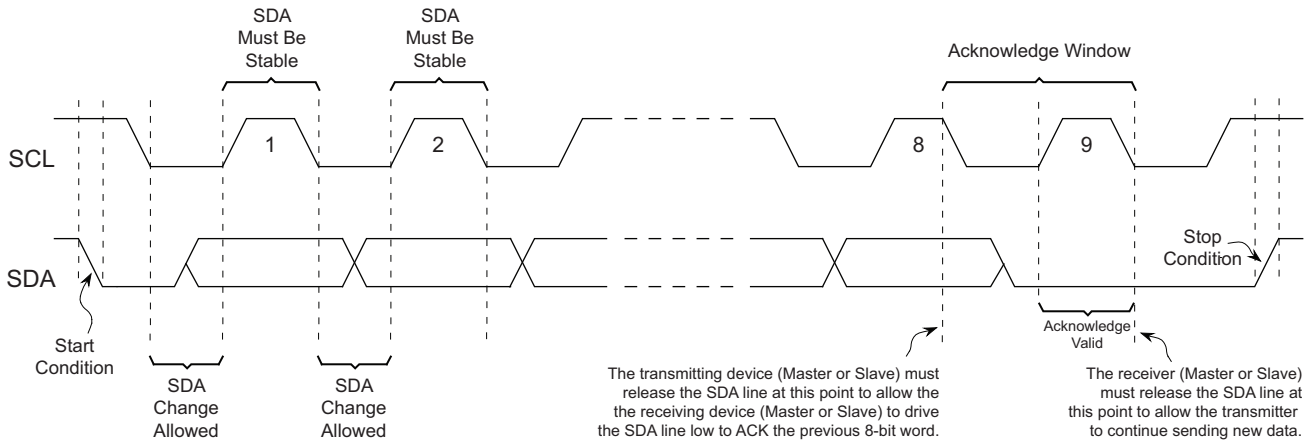
After every byte of data is received, AT30TS01 must acknowledge to the Master that it has successfully received the data byte by responding with an ACK. This is accomplished by the Master first releasing the SDA line and providing the ACK/NACK clock cycle (a ninth clock cycle for every byte). During the ACK/NACK clock cycle, the AT30TS01 must output a Logic 0 (ACK) for the entire clock cycle such that the SDA line must be stable in the Logic 0 state during the entire high period of the clock cycle. Please refer to Figure 4-1 on page 7 for more details.

4.4 No-Acknowledge (NACK)

When the AT30TS01 is transmitting data to the Master, the Master can indicate that it is done receiving data and wants to end the operation by sending a NACK response to the AT30TS01 instead of an ACK response. This is accomplished by the Master outputting a Logic 1 during the ACK/NACK clock cycle, at which point the AT30TS01 will release the SDA line so that the Master can then generate a Stop condition.

In addition, the AT30TS01 can use a NACK to respond to the Master instead of an ACK for certain invalid operation cases such as an attempt to Write to a read-only register (e.g. an attempt to Write to the Temperature Register).

Figure 4-1. Start, Stop, and ACK



4.5 Standby Mode

The AT30TS01 incorporates a low-power Standby Mode which is enabled:

- Upon power-up *or*
- After the receipt of the Stop condition and the completion of any internal operations.

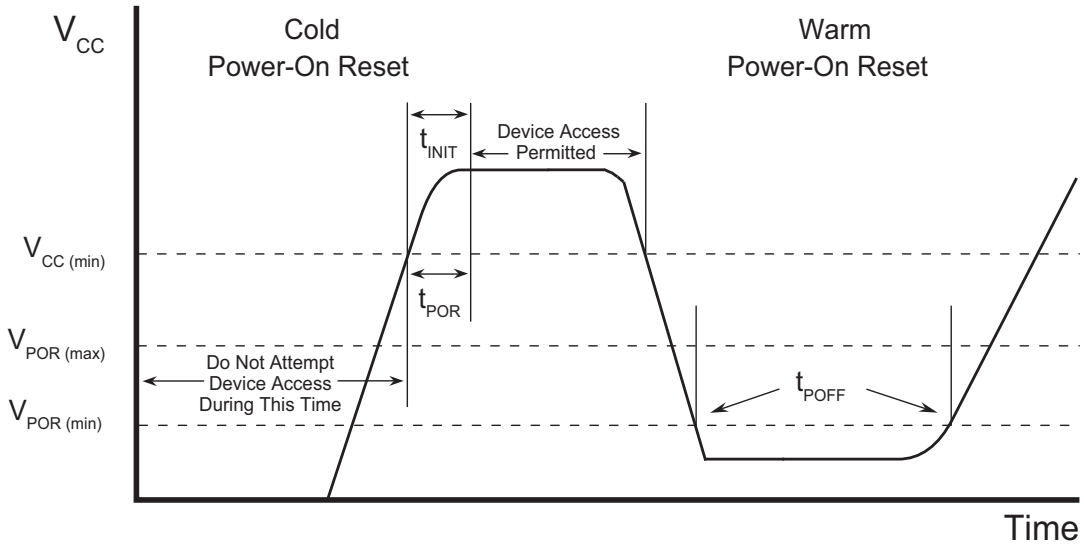
4.6 Device Reset and Initialization

The AT30TS01 incorporates an internal Power-On Reset (POR) circuit to help prevent inadvertent operations during power-up and power-down cycles. On a cold power-up, the supply voltage must rise monotonically between $V_{POR(max)}$ and $V_{CC(min)}$ without any ring back to ensure a proper power-up (see Figure 4-2 on page 8). Once the supply voltage has passed the $V_{POR(min)}$ threshold, the device's internal reset process is initiated. Completion of the internal reset process occurs within the t_{INIT} time listed in Table 4.6.1 on page 8. Upon completion of the internal reset process, the device will have the following power-on default conditions:

- Temperature sensor starts monitoring temperature continuously.
- Pointer Register = 00h
- Upper Limit, Lower Limit, and Critical Alarm Registers are set to 0°C.
- $\overline{\text{EVENT}}$ pin is pulled high by the external pull up resistor.
- Operational mode is Comparator.
- Hysteresis level is set to 0°C.
- $\overline{\text{EVENT}}$ pin polarity is set low.
- $\overline{\text{EVENT}}$ output is disabled and not asserted.

Table 6-1 on page 12 shows the power-on register default values. The Upper Limit, Lower Limit, Critical Alarm, and Configuration Registers should be programmed to their user desired values before the temperature sensor can properly function. Before selecting the device and issuing protocol, a valid and stable supply voltage must be applied and no protocol should be issued to the device for the time specified by the t_{INIT} parameter. The supply voltage must remain stable and valid until the end of the protocol transmission.

Figure 4-2. Power-Up Timing



4.6.1 Power-Up Conditions

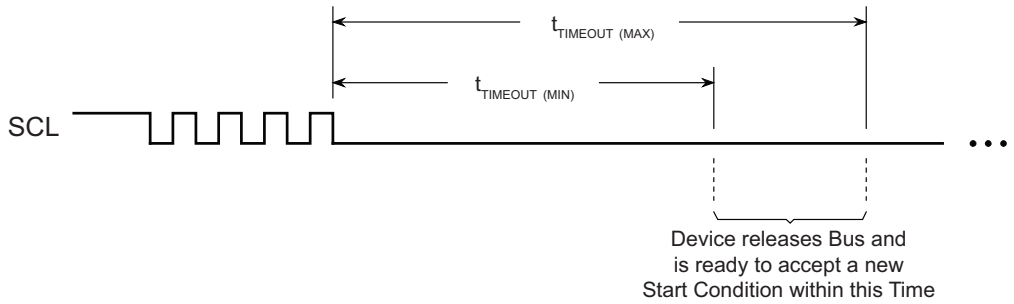
Table 4-1. Power-Up Conditions

Symbol	Parameter	Min	Max	Units
t_{POR}	Power-on Reset Time		10	ms
v_{PON}	Power-on Reset Threshold	1.6		V
v_{POFF}	Power-off Threshold for Warm Power-on Cycle		0.9	V
t_{POFF}	Warm Power Cycle Off Time	1		ms
t_{INIT}	Time from Power-On to First Command	2		ms

4.7 Timeout

The AT30TS01 supports the industry standard bus Timeout feature operations to help prevent potential system bus hang-ups. The device resets its serial interface and stops driving the bus (lets SDA float high) if the SCL pin is held low for more than the minimum Timeout (t_{OUT}) specification. The AT30TS01 is ready to accept a new Start condition before the maximum t_{OUT} has elapsed (see Figure 4-3). This feature does require a minimum SCL clock speed of 10kHz to avoid any timeout issues.

Figure 4-3. Timeout



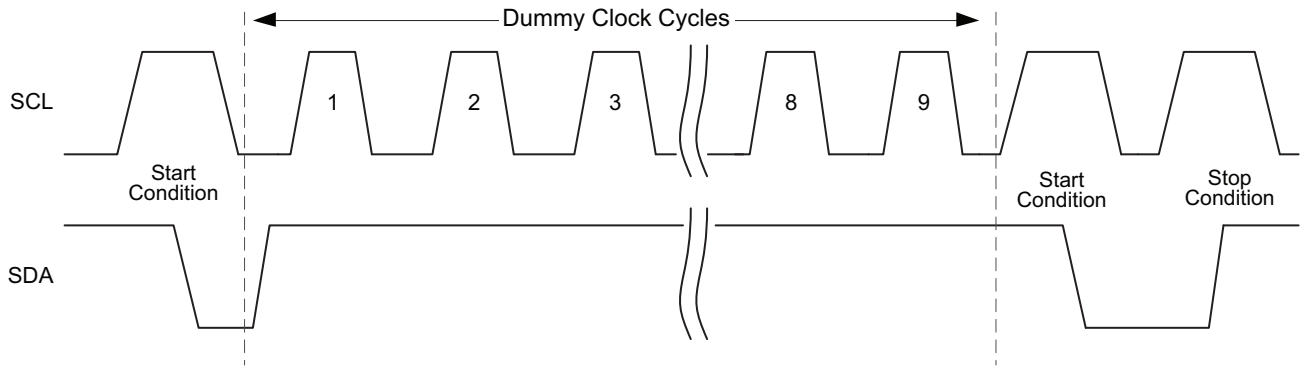
4.8 2-wire Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be reset by following these steps:

1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start condition followed by Stop condition as shown in below.

The device should be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

Figure 4-4. 2-wire Software Reset



5. Device Addressing

The AT30TS01 requires a 7-bit device address and a Read/Write select bit following a Start condition from the Master to initiate communication with either the temperature sensor. The device address byte is comprised of a 4-bit device type identifier followed by three device address bits (A2, A1,and A0) and a R/$\overline{W}$ bit and is clocked by the Master on the SDA pin with the Most Significant bit first. The AT30TS01 responds to a unique device type identifier of `0011b` and is necessary to select the device for reading or writing. See the table below.

Table 5-1. AT30TS01 Device Address Byte

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Function	**Device Type Identifier**				**Device Address**			**Read/Write**
Temperature Sensor	0	0	1	1	A2	A1	A0	R/$\overline{W}$

The software device address bits (A2, A1, and A0) must match their corresponding hard-wired device address inputs (A_2, A_1 and A_0) allowing up to eight devices on the bus at the same time. See the table below. The eighth bit of the address byte is the R/$\overline{W}$ operation selection bit. A Read operation is selected if this bit is a Logic 1, and upon a compare of the device address byte, the AT30TS01 outputs an ACK during the ninth clock cycle. If a compare is not true, the device outputs a NACK during the ninth clock cycle and returns the device to the low-power Standby Mode.

Table 5-2. Device Address Combinations

Software Device Address Bits	Hard-wired Device Address Inputs		
A2, A1, A0	**A_2**	**A_1**	**A_0**
0 0 0	GND	GND	GND
0 0 1	GND	GND	V_{CC}
0 1 0	GND	V_{CC}	GND
0 1 1	GND	V_{CC}	V_{CC}
1 0 0	V_{CC}	GND	GND
1 0 1	V_{CC}	GND	V_{CC}
1 1 0	V_{CC}	V_{CC}	GND
1 1 1	V_{CC}	V_{CC}	V_{CC}

6. Temperature Sensor

6.1 Functional Description

The temperature sensor consists of a Delta-Sigma Analog to Digital Converter (ADC) with a band gap type temperature sensor that monitors and updates its temperature measurement at least sixteen times per second converting the temperature readings into digital data bits and latching them into the Temperature Register that can be read via the 2-wire I^2C FM+ serial interface.

The device communicates over a 2-wire I^2C FM+ interface with a Master consisting of a SCL and a Serial Bidirectional Data Bus (SDA) with clock frequencies up to 1MHz. The Master generates the SCL signal and is used by the AT30TS01 to receive and send serial data on the SDA line with the Most Significant bit transferred first. A pull-up resistor is required on the SDA pin since it has an open drain configuration.

6.1.1 $\overline{\text{EVENT}}$ Output

The $\overline{\text{EVENT}}$ pin has three operating modes depending on the configuration settings:

- Interrupt Mode
- Comparator Mode
- Critical Alarm (Crit_Alarm) Mode

While in Interrupt Mode, once a temperature reaches a boundary limit, the AT30TS01 asserts the $\overline{\text{EVENT}}$ pin. The $\overline{\text{EVENT}}$ pin remains asserted until the system clears the interrupt by writing a Logic 1 to the EVTCLR bit 5 in the Configuration Register. When the temperature drops below specified limits, the device returns back to either Interrupt or Comparator Mode as programmed in the Configuration Register's EVTMOD bit 0.

In Comparator Mode, the $\overline{\text{EVENT}}$ pin remains asserted until the error condition that caused the pin to be asserted no longer exists, and the $\overline{\text{EVENT}}$ pin clears itself. In the Crit_Alarm Mode, when the measured temperature exceeds Crit_Alarm limit, the $\overline{\text{EVENT}}$ pin remains asserted until the temperature drops below the Crit_Alarm limit minus hysteresis (see Figure 6-1 on page 16). All event thresholds use hysteresis as programmed in the Configuration Register.

6.1.2 Alarm Window

The Alarm Window consists of the Upper Limit Register and Lower Limit Register. The Upper Limit Register holds the upper temperature trip point, and the Lower Limit Register holds the lower temperature trip point. After the $\overline{\text{EVENT}}$ pin control is enabled, the $\overline{\text{EVENT}}$ output is triggered upon entering and exiting from this window.

6.2 Register Descriptions

This section describes all the temperature sensor registers that are used in the AT30TS01. The AT30TS01 contains several registers that are user accessible and/or programmable and utilized for latching the temperature readings, storing high, low, and critical temperature limits, configuring the temperature sensor performance, and reporting temperature sensor status.

These registers include a Capability Register, Configuration Register, Upper Limit Register, Lower Limit Register, Critical Alarm Register, Temperature Register, Manufacturer Identification Register, and a Device Identification/Device Revision Register.

The AT30TS01 utilizes an 8-bit Pointer Register to access the 16-bit registers. Table 6-1 indicates the Write/Read access capability for each register.

Note: Reading from a write-only register results in reading Logic 0 data, and writing to a read-only register has no impact even though the write sequence is acknowledged by the device.

Table 6-1. Registers

Register	Address	Read/Write	Section	Power-On Default
Pointer Register	N/A	$\overline{W}$	6.2.1	00h
Capability Register	00h	R	6.2.2	007Fh
Configuration Register	01h	R/$\overline{W}$	6.2.3	0000h
Upper Limit Register	02h	R/$\overline{W}$	6.2.4	0000h
Lower Limit Register	03h	R/$\overline{W}$	6.2.5	0000h
Critical Alarm Register	04h	R/$\overline{W}$	6.2.6	0000h
Temperature Register	05h	R	6.2.7	N/A
Manufacturer I.D. Register	06h	R	6.2.8	1114h
Device I.D./Device Revision Register	07h	R	6.2.9	3200h
Reserved (1)	08h to 0Fh	R/$\overline{W}$	N/A	N/A

Note: 1. Write operations to reserve registers should be avoided as it may cause undesirable results.

6.2.1 Pointer Register (8-bit Write Only, Address = N/A)

The AT30TS01 utilizes a Pointer Register to select and access all the data registers shown on Table 6-1. The Pointer Register is an 8-bit write-only register as shown in the below table. The power-on default value is 00h which is the address location for the Capability Register.

Table 6-2. Pointer Register

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	Pointer Register Value							
R/W	W	W	W	W	W	W	W	W
Default Value	0	0	0	0	0	0	0	0

6.2.2 Capability Register (16-bit Read-only, Address = 00h)

This register is a 16-bit read-only register used to specify the functional capabilities of the temperature sensor. The AT30TS01 is capable of measuring temperature with ±1°C over the active range and ±2°C over the monitor range. The Capability Register functions are described in Table 6-3 and Table 6-4.

Table 6-3. Capability Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	RFU							
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	EVSD	TMOUT	RFU	TPRES		RANGE	SACC	ICAP
Default Value	0	1	1	1	1	1	1	1
R/W Access	R	R	R	R	R	R	R	R

Table 6-4. Capability Register Bit Description

Bit	Symbol	Description
15:8	RFU	***Reserved*** for ***Future Use.*** Read as Logic 0.
7	EVSD	**Event Output Status During Shutdown Mode**: 0 = The $\overline{\text{EVENT}}$ output freezes in its current state when entering shutdown. Upon exiting shutdown, the EVENT output remains in theprevious state until the next thermal sample is taken, or possibly sooner if $\overline{\text{EVENT}}$ pin is programmed for comparator mode.
6	TMOUT	Timeout: 1 = Bus Timeout supported within the range 25 to 35ms.
5	RFU	***Reserved*** for ***Future Use.*** Read as Logic 1.
4:3	TPRES	Temperature Resolution: 11 = 0.0625°C (12-bit) only.
2	RANGE	1 = Can read temperatures below 0°C and sets appropriate sign bit.
1	SACC	Supported Accuracy: 1 = Supports accuracy of ±1°C over the active range (75°C to 95°C) and 2°C over the (40°C to 125°C) range.
0	ICAP	Interrupt Capability: 1 = Supports Interrupt capabilities.

6.2.3 Configuration Register (16-bit Read/Write, Address = 01h)

The AT30TS01 incorporates a 16-bit Configuration Register allowing the user to set key operational features of the temperature sensor. The Configuration Register functions are described in Table 6-5 and Table 6-6.

Table 6-5. Configuration Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	RFU					HYSTENB		SHTDWN
Default Value	0	0	0	0	0	0	0	0
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	CRTALML	WINLOCK	EVTCLR	EVTSTS	EVTOUT	CRITEVT	EVTPOL	EVTMOD
Default Value	0	0	0	0	0	0	0	0
R/W Access	R/W	R/W	W	R	R/W	R/W	R/W	R/W

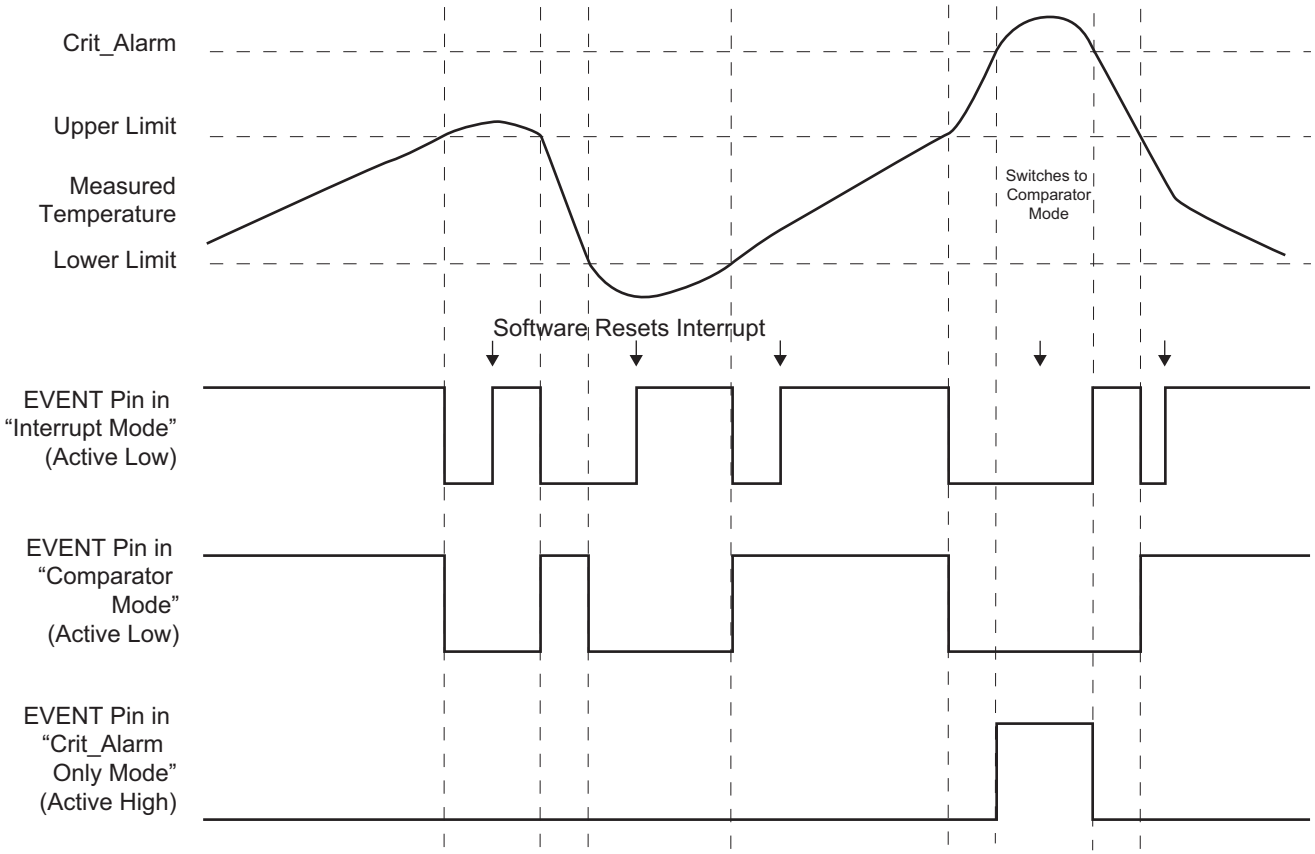
Table 6-6. Configuration Register Bit Description

Bit	Symbol	Description
15:11	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.
10:9	HYSTENB	Hysteresis Enable: 00 = 0°C Disable hysteresis (Power-on default) 01 = 1.5°C Enable hysteresis 10 = 3.0°C Enable hysteresis 11 = 6.0°C Enable hysteresis The purpose of these bits is to control the hysteresis applied to the temperature limit trip point boundaries. The above hysteresis applies to all limits when temperature drops below the user specified temperature limit trip points. Note: Hysteresis applies to decreasing temperature only. Once the temperature is above a given threshold, the temperature must drop below the boundary limit minus hysteresis in order for a Comparator $\overline{\text{EVENT}}$ to be cleared. Example: If these two bits are set to 01 for 1.5°C and the Upper Limit is set to 85°C, as temperature rises above 85°C, bit 14 of the Temperature Register is set to a Logic 1. Bit 14 remains set until the temperature drops below the threshold (85°C) minus the hysteresis value(83.5°C). Note: Hysteresis is also applied to the $\overline{\text{EVENT}}$ pin functionality. This bit cannot be changed if the Crit_Alarm or Alarm Window Lock bits is set.
8	SHTDWN	Shutdown Mode: 0 = The temperature sensor is enabled for continuous conversion (power-on default). 1 = The temperature sensor is disabled. To save power in Shutdown Mode, the temperature sensor is not active and does not generate interrupts or update the temperature data. This bit cannot be set to a Logic 1 if either of the Crit_Alarm or Alarm Window Lock bits is set; however, it can be cleared at any time. The device responds to protocol commands, and the bus timeout is active when in Shutdown Mode.

Table 6-6. Configuration Register Bit Description (Continued)

Bit	Symbol	Description
7	CRTALML	Crit_Alarm Lock bit: 0 = The Crit_Alarm Register can be updated (power-on default). 1 = The Crit_Alarm Register is locked and cannot be updated. This bit locks the Critical Alarm Register from being updated. Once set, it can only be cleared to a Logic 0 by an internal Power-On Reset.
6	WINLOCK	Alarm Window Lock bit: 0 = The Upper Limit and Lower Limit Registers can be updated (power-on default). 1 = The Upper and Lower Limit Registers are locked and cannot be updated. Once set, it can only be cleared to a Logic 0 by an internal Power-On Reset.
5	EVTCLR	$\overline{\text{EVENT}}$ Clear: 0 = Has no effect (power-on default). 1 = Clears (releases) the active $\overline{\text{EVENT}}$ pin in Interrupt Mode. This bit clears the $\overline{\text{EVENT}}$ pin after it has been enabled. This bit is a write-only bit, is read as a Logic 0, and is ignored when in Comparator Mode.
4	EVTSTS	$\overline{\text{EVENT}}$ Pin Output Status: 0 = The $\overline{\text{EVENT}}$ output is not asserted by the device (power-on default). 1 = The $\overline{\text{EVENT}}$ output is asserted due to a limit or alarm condition.
3	EVTOUT	$\overline{\text{EVENT}}$ Output Control: 0 = The $\overline{\text{EVENT}}$ output is disabled and does not generate interrupts (power-on default). 1 = The $\overline{\text{EVENT}}$ output is enabled. This bit cannot be altered if the Crit_Alarm or the Alarm Window Lock bits is set.
2	CRITEVT	Critical Temperature only: 0 = The $\overline{\text{EVENT}}$ output is asserted if the measured temperature is above the Upper Limit or Critical Alarm, or is below the Lower Limit (power-on default). 1 = The $\overline{\text{EVENT}}$ output is asserted only for a Critical Alarm violation when the temperature is greater then the Crit_Alarm. This bit cannot be altered if the Alarm Window Lock bit is set.
1	EVTPOL	$\overline{\text{EVENT}}$ Polarity: 0 = The $\overline{\text{EVENT}}$ pin is active low (power-on default). 1 = The $\overline{\text{EVENT}}$ pin is active high. This bit cannot be altered if the Crit_Alarm or the Alarm Window Lock bit is set. A pull-up resistor is required on this pin to achieve the Logic 1 state.
0	EVTMOD	$\overline{\text{EVENT}}$ Mode: 0 = The $\overline{\text{EVENT}}$ pin operates in Comparator Mode (power-on default). 1 = The $\overline{\text{EVENT}}$ pin operates in Interrupt Mode. This bit cannot be altered if the Crit_Alarm or the Alarm Window Lock bit is set.

Figure 6-1. $\overline{\text{EVENT}}$ Pin Mode Functionality



6.2.4 Upper Limit Register (16-bit Read/Write, Address = 02h)

The Upper Limit Register holds the user programmed upper temperature boundary trip point in 2's complement format (0.0625°C resolution) that can be utilized to monitor the temperature in an operating window between the Upper Limit Register and the Lower Limit Register settings (see Table 6-7 and Table 6-9). When the temperature increases above this trip point, drops below, or is equal to the trip point (minus any hysteresis set), then the $\overline{\text{EVENT}}$ pin is asserted (if enabled). This register is read-only if the Alarm Window Lock (WINLOCK) bit six in the Configuration Register is set to a Logic 1.

Table 6-7. Upper Limit Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	RFU			SIGN	ALMWINH			
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R/W	R/W	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	ALMWINH						RFU	
Default Value	0	0	0	0	0	0	0	0
R/W Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 6-8. Upper Limit Register Bit Description

Bit	Symbol	Description
15:13	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.
12	SIGN	Sign bit: 0 = The temperature is greater than or equal to 0°C. 1 = The temperature is less than 0°C.
11:2	ALMWINH	Upper Limit temperature bits: • Represented in 2's complement format. • Read-only access if Alarm Window is locked (Configuration Register bit 6 high). • R/W access if the Alarm Window is unlocked.
0:1	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.

6.2.5 Lower Limit Register (16-bit Read/Write, Address = 03h)

The Lower Limit Register holds the user programmed lower temperature boundary trip point in 2's complement format (0.0625°C resolution) that can be utilized to monitor the temperature in an operating window (see Table 6-7 and Table 6-9). When the temperature decreases below this trip point minus any hysteresis set or increases to meet or exceed this trip point, then the $\overline{\text{EVENT}}$ pin is asserted (if enabled).

This register becomes read-only if the Alarm Window Lock (WINLOCK) bit 6 in the Configuration Register is set to a Logic 1.

Table 6-9. Lower Limit Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	RFU			SIGN	ALMWINL			
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R/W	R/W	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	ALMWINL						RFU	
Default Value	0	0	0	0	0	0	0	0
R/W Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 6-10. Lower Limit Register Bit Description

Bit	Symbol	Description
15:13	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.
12	SIGN	Sign bit: 0 = The temperature is greater than or equal to 0°C. 1 = The temperature is less than 0°C.
11:2	ALMWINL	Lower limit temperature bits: • Represented in 2's complement format. • Read-only access if Alarm Window is locked (Configuration Register bit 6 high). • R/W access if the Alarm Window is unlocked.
0:1	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.

6.2.6 Critical Alarm Register (16-bit Read/Write, Address = 04h)

The Critical Alarm Register holds the user programmed Critical Alarm temperature boundary trip point in 2's complement format (0.0625°C resolution) that can be utilized to monitor the temperature (see Table 6-11 and Table 6-12). When the temperature increases above this trip point, the $\overline{\text{EVENT}}$ pin is asserted (if enabled). It remains asserted until the temperature decreases below or equal to the trip point minus any hysteresis set. This register becomes read-only if the Critical Alarm Lock Bit (CRTALML) bit 7 in the Configuration Register is set to a Logic 1.

Table 6-11. Critical Alarm Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	RFU			SIGN	CRITEVT			
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R/W	R/W	R/W	R/W	R/W
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	CRITEVT						RFU	
Default Value	0	0	0	0	0	0	0	0
R/W Access	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Table 6-12. Critical Alarm Register Bit Description

Bit	Symbol	Description
15:13	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.
12	SIGN	Sign bit: 0 = The temperature is greater than or equal to 0°C. 1 = The temperature is less than 0°C.
11:2	CRITEVT	Critical Alarm temperature bits: • Represented in 2's complement format. • Read-only access if Alarm Window is locked (Configuration Register bit 6 high). • R/W access if the Alarm Window is unlocked.
0:1	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.

6.2.7 Temperature Register (16-bit Read-only, Address = 05h)

The Temperature Register holds the internal temperature measurement data represented in 2's complement format allowing for resolution equal to 0.0625°C (Least Significant bit). The upper three bits (15, 14, and 13) of the Temperature Register indicates the trip status of the current temperature and most important, are not affected by the status of the output of the $\overline{\text{EVENT}}$ pin (see Table 6-13 and Table 6-14).

Table 6-13. Temperature Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	CRITHIGH	ALMHIGH	ALMLOW	SIGN	128°C	64°C	32°C	16°C
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	8°C	4°C	2°C	1°C	0.5°C	0.25°C	0.125°C	0.0625°C
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R	R	R	R	R

Table 6-14. Temperature Register Bit Description

Bit	Symbol	Description
15	CRITHIGH	0 = The temperature is less than the Critical Alarm Register setting. 1 = The temperature is greater than or equal to Critical Alarm Register setting. When this bit is set to a Logic 1, it automatically clears once the measured temperature decreases below or is equal to the trip point minus any hysteresis set.
14	ALMHIGH	0 = The temperature is below the Upper Limit Register setting. 1 = The temperature is above the Upper Limit Register setting. When the bit is set to a Logic 1, it automatically clears once the measured temperature decreases below or is equal to the trip point minus any hysteresis set.
13	ALMLOW	0 = The temperature is above the Lower Limit Register setting. 1 = The temperature is below the Lower Limit Register setting. When the bit is set to a Logic 1, it automatically clears once the measured temperature increases above or is to equal to the trip point.
12	SIGN	Sign bit: 0 = The temperature is greater than or equal to 0°C. 1 = The temperature is less than 0°C.
11:1	TEMP	Temperature bits: • Represented in 2's complement format. • The encoding of bits B11 through B2 is the same as in the limit and alarm registers.
0	RFU	***Reserved*** for ***Future Use***. Read as Logic 0.

6.2.7.1 Temperature Register Format

This section clarifies the Temperature Register format and temperature bit value assignments utilized for temperature for the following registers: Upper Limit, Lower Limit, Critical Alarm, and Temperature. The temperatures expressed in the Upper Limit, Lower Limit, Critical Alarm, and Temperature Registers are indicated in 2's complement format. In each of the temperature limit registers, bits 12 through bit 1 are utilized for temperature settings, or in the case of the Temperature Register, holds the internal temperature measurement with bits 12 through bit 0 allowing 12-bit (0.0625ºC) resolution.

Table 6-15 indicates the Temperature Register's assigned bit values utilized for temperature and shows examples for the Temperature Register bit values for various temperature readings.

Table 6-15. Temperature Register Format

Position	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Value	SIGN	128°C	64°C	32°C	16°C	8°C	4°C	2°C	1°C	0.5°C	0.25°C	0.125°C	0.0625°C

Table 6-16. Temperature Register Examples

Temperature Register Value Examples	
Temperature	**Binary (Bit 15 – Bit 0)**
+125°C	xxx0 0111 1101 000x
+99.75°C	xxx0 0110 0011 110x
+85°C	xxx0 0101 0101 000x
+39°C	xxx0 0010 0111 000x
+15.75°C	xxx0 0000 1111 110x
+0.25°C	xxx0 0000 0000 010x
0°C	xxx0 0000 0000 000x
-0.25°C	xxx1 1111 1111 110x
-1°C	xxx1 1111 1110 000x
-20°C	xxx1 1110 1100 000x

6.2.8 Manufacturer ID Register (16-bit Read-only, Address = 06h)

The Manufacturer ID Register contains the PCI SIG number assigned to Atmel (1114h) as shown in Table 6-17.

Table 6-17. Manufacturer ID Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	Manufacturer ID							
Default Value	0	0	0	1	0	0	0	1
R/W Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	Manufacturer ID							
Default Value	0	0	0	1	0	1	0	0
R/W Access	R	R	R	R	R	R	R	R

6.2.9 Device ID Register (16-bit Read-only, Address = 07h)

The upper or high order byte is used to specify the device identification, and the low byte is used to specify the device revision. The Device ID for the AT30TS01 is 3200h (see Table 6-18).

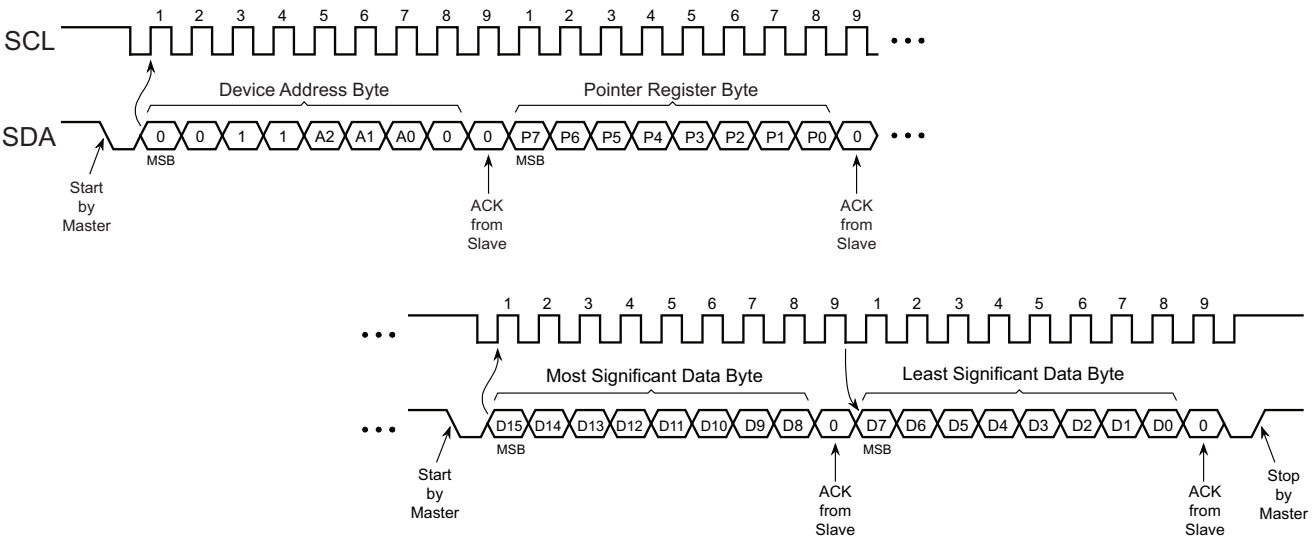
Table 6-18. Device ID Register Bit Distribution

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Symbol	Device ID							
Default Value	0	0	1	1	0	0	1	0
R/W Access	R	R	R	R	R	R	R	R
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Symbol	Device Revision							
Default Value	0	0	0	0	0	0	0	0
R/W Access	R	R	R	R	R	R	R	R

6.3 Temperature Sensor Write Operations

Writing to the AT30TS01 Temperature Register is accomplished through a modified write operation for two data bytes. To maintain 2-wire compatibility, the 16-bit registers are accessed through a Pointer Register requiring the TS write sequence to include a Pointer Register byte following the device address byte to write the two data bytes. Figure 6-2 illustrates the entire write transaction.

Figure 6-2. Temperature Sensor Register Write Operation



6.4 Temperature Sensor Read Operations

Reading data from the temperature sensor may be accomplished in one of two ways:

- If the location latched in the Pointer Register is correct (for normal operation, it is expected the same address is read repeatedly to read the temperature from the Temperature Register), the Register Pointer Word Read sequence should be utilized as shown in Figure 6-3. To perform a Register Pointer Word Read, the Master transmits a Start condition followed by a device address byte with the R/$\overline{W}$ select bit to a Logic 1. The AT30TS01 should respond with an ACK and transmit the most significant data byte. The Master should send an ACK followed by the device transmitting the least significant data byte. To end the read operation, the Master sends a NACK followed by a Stop condition.
- If it is desired to read a Random Register or simply change to read a different register from the temperature sensor, then the Preset Pointer Register Word Read protocol sequence should be followed and is shown in Figure 6-4. The Preset Pointer Register Word Read sequence allows the Pointer Register to be preloaded with the correct register address to gain access to the desired register to be read. To perform a Preset Pointer Register Word Read, the Master transmits a Start condition followed by a device address byte (with the R/$\overline{W}$ select bit to a Logic 0) and a Pointer Register byte to the AT30TS01. Once the device address and Pointer Register bytes are clocked in and acknowledged by the AT30TS01, the Master must generate another Start condition. The Master transmits another device address byte (with the R/$\overline{W}$ select bit to a Logic 1) followed by an ACK by the AT30TS01 and the device transmitting the most significant data byte. The Master should send a ACK followed by the device transmitting the least significant data byte. To end the read operation, the Master should send a NACK followed by a Stop condition.

Figure 6-3. Register Pointer Word Read

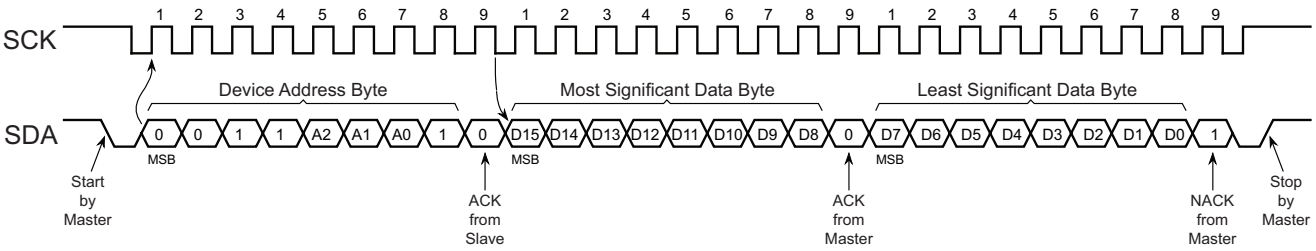
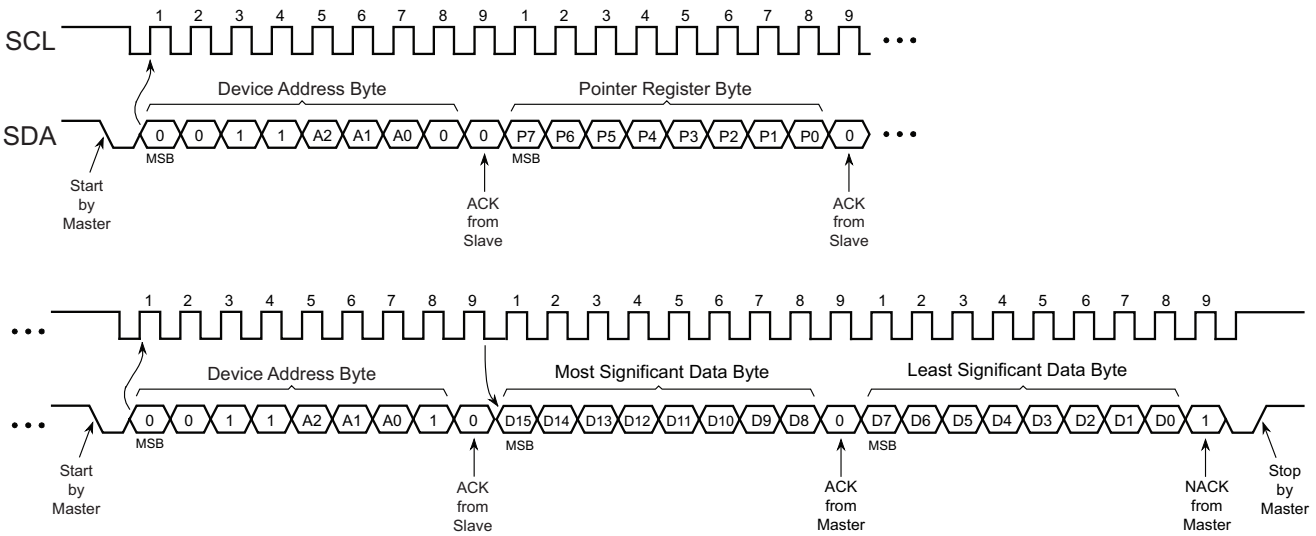


Figure 6-4. Preset Pointer Register Word Read



7. Electrical Specifications

7.1 Absolute Maximum Ratings

Temperature under Bias. . . . . -40°C to +125°C

Storage Temperature . . . . . -65°C to +150°C

Supply voltage
with respect to ground . . . . . -0.5V to +4.3V

A_0 Pin . . . . . -0.5V to +12.0V

All other input voltages
with respect to ground . . . . . -0.5V to V_{CC} + 0.5V

$\overline{EVENT}$ Pin . . . . . -0.5V to V_{CC} + 0.3V

All other output voltages
with respect to ground . . . . . -0.5V to V_{CC} + 0.5V

*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these ratings or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.

Pull-up voltages applied to the $\overline{EVENT}$ Pin that exceed the “Absolute Maximum Ratings” may forward bias the ESD protection circuitry. Doing so may result in improper device function and may corrupt temperature measurements.

7.2 DC Characteristics

Table 7-1. DC Characteristics

Applicable over recommended operating range: T_{AI} = -20°C to +125°C, V_{CC} = 1.7V to 3.6V (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.7		3.6	V
I_{CC1}	Temp Sensor	V_{CC} = 3.6V			0.2	0.5	mA
I_{SB}	Standby Current	V_{CC} = 1.7V	V_{IN} = V_{CC} or V_{SS}		1.6	3.0	µA
		V_{CC} = 3.6V	V_{IN} = V_{CC} or V_{SS}		1.6	4.0	µA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}			0.1	2.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}			0.1	2.0	µA
V_{IL}	Input Low Level(1)			-0.5		0.3 * V_{CC}	V
V_{IH}	Input High Level(1)			0.7 * Vcc		Vcc + 0.5	V
V_{OL1}	Low-Level Output Voltage Open-Drain	V_{CC} > 2V	I_{OL} = 3mA			0.4	V
V_{OL2}		V_{CC} ≤ 2V	I_{OL} = 2mA			0.2 * V_{CC}	V
I_{OL}	Low-Level Output Current	V_{OL} = 0.4V	Freq ≤ 400kHz	3.0			mA
		V_{OL} = 0.6V	Freq ≤ 400kHz	6.0			mA
		V_{OL} = 0.4V	Freq > 400kHz	20.0			mA
V_{HYST1}	Input Hysteresis (SDA, SCL)	V_{CC} < 2V		0.10 * V_{CC}			V
V_{HYST2}	Input Hysteresis (SDA, SCL)	V_{CC} ≥ 2V		0.05 * V_{CC}			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

7.3 AC Characteristics

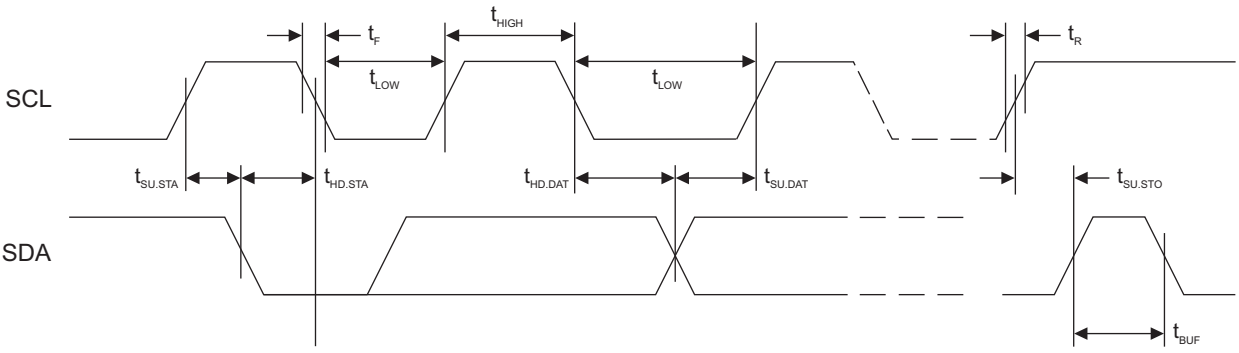
Table 7-2. AC Characteristics

Applicable over recommended operating range: T_{AI} = -20°C to +125°C, V_{CC} = 1.7V to 3.6V, CL = 1 TTL Gate and 100µF (unless otherwise noted).

Symbol	Parameter	$V_{CC} \geq 1.7V$						Units
		100kHz		400kHz		1000kHz		
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock Frequency, SCL	10[2]	100	10[2]	400	10[2]	1000	kHz
t_{LOW}	Clock Pulse Width Low	4,700		1,300		500		ns
t_{HIGH}	Clock Pulse Width High	4,000		600		260		ns
t_I	Noise Suppression Time		50		50		50	ns
t_{BUF}	Time the bus must be free before a new transmission can start.[1]	4,700		1,300		500		ns
$t_{HD.STA}$	Start Hold Time	4,000		600		260		ns
$t_{SU.STA}$	Start Set-up Time	4,700		600		260		ns
$t_{HD.DI}$	Data In Hold Time	0		0		0		ns
$t_{SU.DAT}$	Data In Set-up Time	250		100		50		ns
t_R	Inputs Rise Time[1]		1,000	20	300		120	ns
t_F	Inputs Fall Time[1]		300	20	300		120	ns
$t_{SU.STO}$	Stop Set-up Time	4,000		600		260		ns
$t_{HD.DAT}$	Data Out Hold Time	200	3,450	200	900	0	350	ns
t_{OUT}	Timeout Time	25	35	25	35	25	35	ms

Notes: 1. This parameter is ensured by characterization only.
2. The minimum frequency is specified at 10kHz to avoid activating the timeout feature.

Figure 7-1. SCL: Serial Clock; SDA: Serial Data I/O



7.4 Temperature Sensor Characteristics

Table 7-3. Temperature Sensor Characteristics

Applicable over recommended operating range: T_{AI} = -20°C to +125°C, V_{CC} = 1.7V to 3.6V (unless otherwise noted).

Symbol	Parameter	Test Condition	Freq. ≤ 400kHz			Freq. > 400kHz			Units
			Min	Typ	Max	Min	Typ	Max	
T_{ACC}	TS Accuracy	+75°C < T_A < +95°C		±0.5	±1.0		±0.5	±1.0	°C
		+40°C < T_A < +125°C		±1.0	±2.0		±1.0	±2.0	°C
		-20°C < T_A < +125°C		±2.0	±3.0		±2.0	±3.0	°C
T_{CONV}	TS Conversion Time			75	100		75	100	ms
T_{RES}	TS Resolution				0.0625			0.0625	°C

7.5 Pin Capacitance

Table 7-4. Pin Capacitance[1]

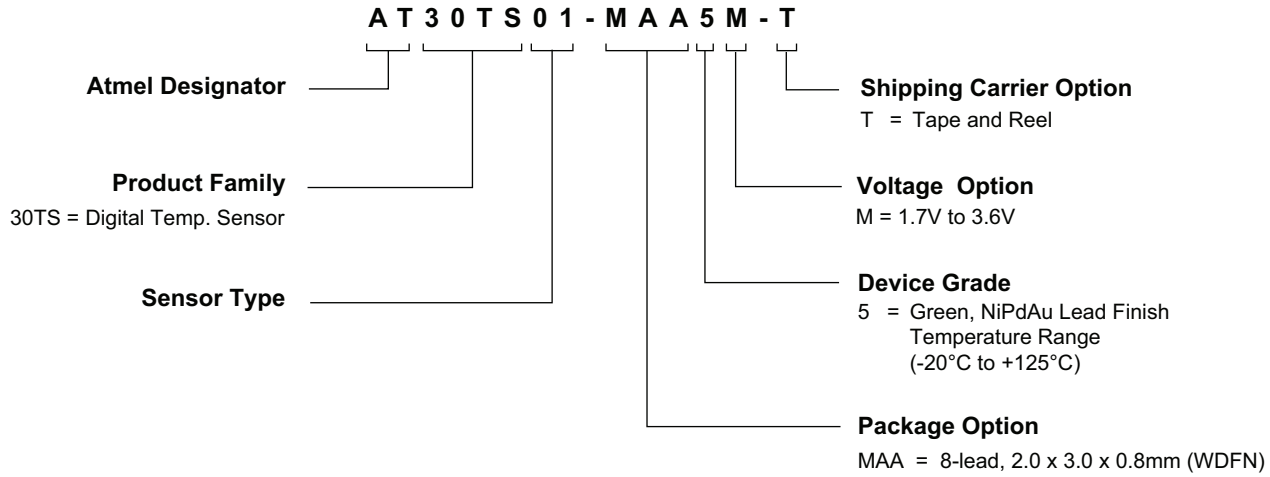
Applicable over recommended operating range from T_A = +25°C, f = 1MHz, V_{CC} = 1.7V to 3.6V.

Symbol	Test condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA, $\overline{EVENT}$)	8	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

Note: 1. This parameter is ensured by characterization only.

8. Ordering Information

8.1 Ordering Code Detail



8.2 Ordering Code Information

Ordering Code[1]	Lead Finish	Package	Operating Voltage	Max. Frequency	Delivery Information		Operational Range
					Form	Quantity	
AT30TS01-MAA5M-T	NiPdAu	8MAA	1.7V to 3.6V	1,000kHz	Tape and Reel	5,000 per Reel	-20°C to 125°C

Note: 1. Consistent with the general semiconductor market trend, Atmel will supply devices with either gold or copper bond wires to increase manufacturing flexibility and ensure a long-term continuity of supply. There is no difference in product quality, reliability, or performance between the two variations.

	Package Type
8MAA	8-lead, 2.0 x 3.0 x 0.8mm, Thermally Enhanced Plastic Very Very Thin Dual Flat No Lead (WDFN)

9. Part Markings

AT30TS01: Package Marking Information

8-lead WDFN

2.0 x 3.0 mm Body



Note 1: ● Designates pin 1

Note 2: Package drawings are not to scale

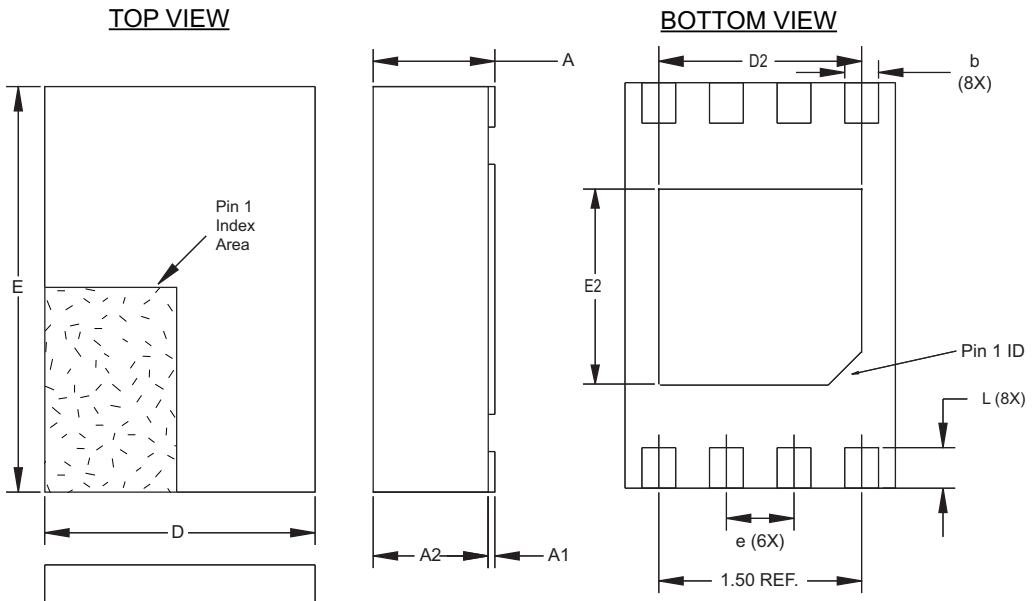
Catalog Number Truncation			
AT30TS01		Truncation Code ###: TA	
Date Codes			**Voltages**
Y = Year	M = Month	WW = Work Week of Assembly	% = Minimum Voltage
5: 2015 9: 2019 6: 2016 0: 2020 7: 2017 1: 2021 8: 2018 2: 2022	A: January B: February ... L: December	02: Week 2 04: Week 4 ... 52: Week 52	M: 1.7V min
Country of Assembly	**Lot Number**		**Grade/Lead Finish Material**
@ = Country of Assembly	AAA...A = Atmel Wafer Lot Number		5: Industrial (-20°C to 125°C) NiPdAu
Trace Code			**Atmel Truncation**
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ			AT: Atmel ATM: Atmel ATML: Atmel

5/4/15

Atmel Package Mark Contact: DL-CSO-Assy_eng@atmel.com	**TITLE** **30TS01SM**, AT30TS01 Package Marking Information	**DRAWING NO.** 30TS01SM	**REV.** A

10. Package Drawings

10.1 8MAA — 8-pad WDFN



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.70	0.75	0.80	
A1	0.00	0.02	0.05	
A2	0.45	0.55	0.65	
A3		2.0 REF		
D	1.90	2.00	2.10	
D2	1.20	-	1.60	
E	2.90	3.00	3.10	
E2	1.20	-	1.60	
b	0.18	0.25	0.30	2
L	0.30	–	0.45	
e		0.50 BSC		

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-229, WCED-3, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.
3. Soldering the large thermal pad is optional, but not recommended. No electrical connection is accomplished to the device through this pad, so if soldered it should be tied to ground

09/11/12

Atmel Package Drawing Contact: packagedrawings@atmel.com	TITLE 8MAA, 8-pad 2.0 x 3.0mm Body, 0.50mm Pitch Very, Very Thin Dual No Lead Package (WDFN) (Sawn)	GPC YRV	DRAWING NO. 8MAA	REV. A

11. Revision History

Doc. Rev.	Date	Comments
8952A	12/2015	Initial document release.

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